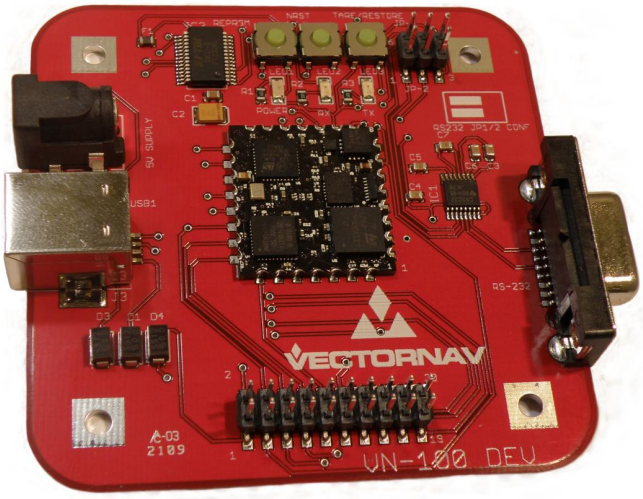
VN-100 Development Board

User Manual



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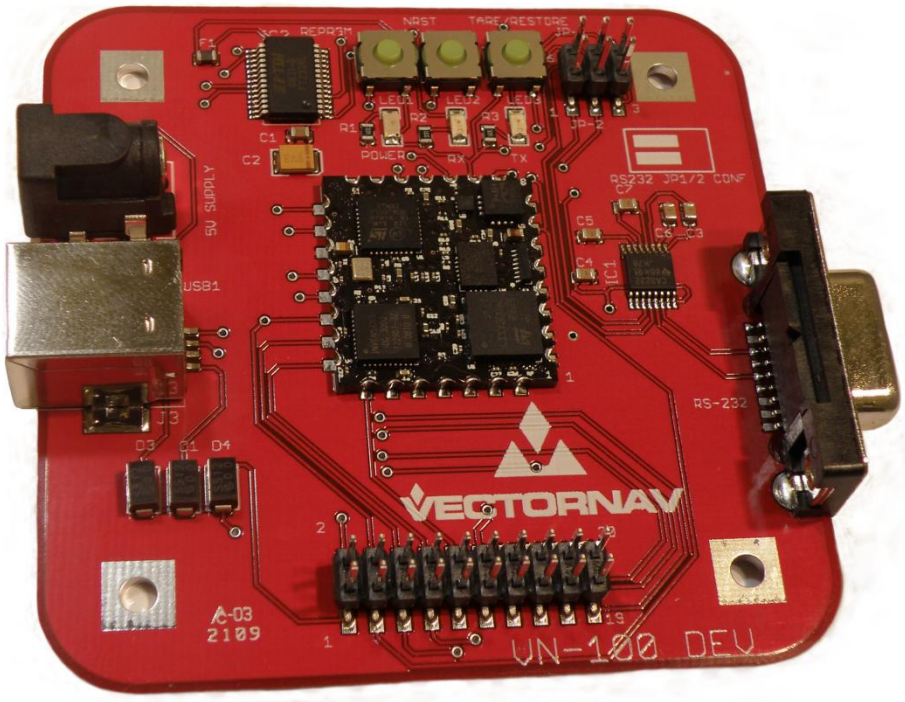
1 Introduction

The VN-100 DEV is a development board for VN-100 attitude and heading reference module. It is designed to provide easy access to the module for development purposes. USB and RS-232 interfaces are provided, along with a header that includes full prototyping access to the VN-100.

The board can be powered by the USB host computer, a 5 V adapter, or through the 20 pin header. A red LED indicates the power status of the board.

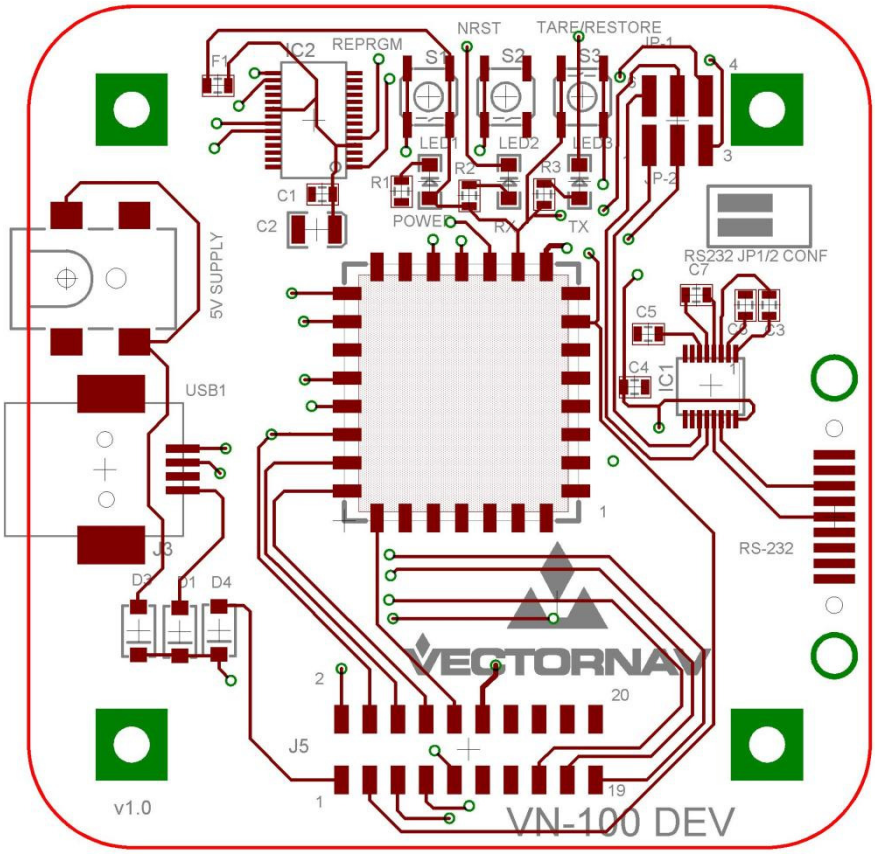
The VN-100 North, East, Down coordinate system is shown in the mechanical drawings section.

Figure 1 – Development Board



2 Board configuration

Figure 2 – Board Layout



2.1 Jacks

2.2 USB

The USB jack is a USB-B port. When connected to a PC the VN-100 DEV board will power up and a RED status LED will be illuminated. Drivers for the USB to UART must be installed for proper operation of this port. These are supplied with the documentation for the board or they can be downloaded at www.vectornav.com.

2.3 DB-9

The DB-9 port provides access to RS-232 level logic. The RS-232 line driver supports speeds up to 1 Mbit. The RS-232 interface requires the VN-100 DEV board to be powered to function properly. The power can be supplied thru the USB port or thru the 5V power jack.

2.4 Power Jack

This is a standard 5V power jack. This powers the board when using the RS-232 interface.

Warning: Do not exceed 6V input power.

2.5 Indicator lights

2.5.1 Red LED

Turns bright red when power is supplied to the board.

2.5.2 Green LED's

These LED's will flash when data is being transferred across USB. When using the RS-232 logic interface, neither the RX nor the TX LED on the silkscreen will flash. This is normal behavior and does not indicate that the board is not receiving/transmitting data.

2.6 Push Buttons

2.6.1 S1/REPRGM

S1 is only used to enable the VN-100 Boot mode. Depressing this switch during power-up, or reset of the VN-100 module will set the VN-100 into boot mode.

2.6.2 S2/NRST

S2 is used for re-setting the VN-100. Depressing S2 at any time while the board is running will reset the VN-100 module.

2.6.3 S3/TARE/RESTORE

S3 is normally used to tare the VN-100. To tare, pulse high for at least 1 µs. During power on or device reset, depressing S3 will cause the module to restore its default factory settings. Because of this, this button cannot be used for tare until at least 10 ms after a power on or reset.

2.7 Jumpers

2.7.1 JP1

JP1 toggles the TX (data leaving the VN-100 module) UART data line. With the jump between pin 1 and pin 2 the TX signal is routed to the RS-232 interface. Setting the jump to pin 2 and pin 3 enables the TX at the USB interface.

2.7.2 JP2

JP2 toggles the RX (data entering the VN-100 module) UART data line. With the jump between pin 5 and pin 6 the RX signal is routed to the RS-232 interface. Setting the jump to pin 4 and pin 5 enables the RX at the USB interface.

2.7.3 J5 – Header

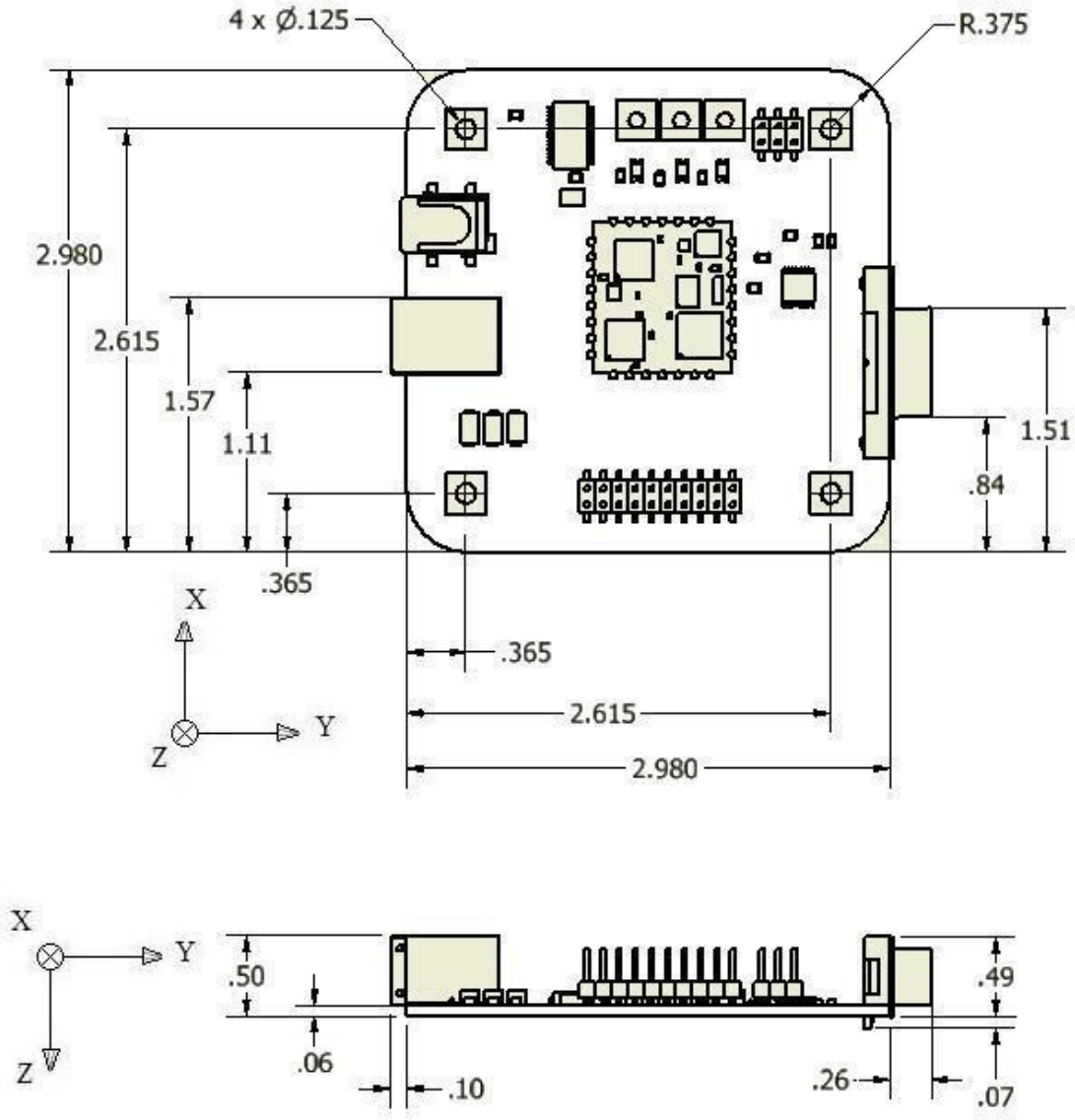
The J5 header provides a complete interface to all the used pins on the VN-100 module.

Table 1 – 20-Pin Header

Pin number	Description	Pin on VN-100	Note:
1	Vcc (3.3-5.5V)	10	Power can only be supplied to the board and VN-100
2	REPRGM	20	
3	TARE/RESTORE	7	
4	NRST	21	
5	ENABLE	11	ON state. Pull low to enter sleep mode
6	Not Used	22	
7	TX	12	Data leaving VN-100 (UART 0/3.0V)
8	SPI_CS	23	SPI slave select
9	RX	13	Data entering VN-100 (UART 0/3.0V)
10	Not Used	24	
11	Not Used	15	
12	DR_INT	9	Data Ready Interrupt. Will pulse low for 500 us
13	Not Used	14	
14	GND	(1-4)	
15	SPI_SCK	16	SPI clock
16	GND	(1-4)	
17	SPI_MOSI	17	SPI master output/slave input
18	GND	(1-4)	
19	SPI_MISO	19	SPI master input/slave output
20	GND	(1-4)	

3 Mechanical Drawings

Figure 3 – Board Dimensions



4 Revision history

Table 2 – Revision History

Date	Revision	Changes
Jun-05-2009	1.0.0	Initial release.
Oct-06-2009	1.1.0	New document format.

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