

Select:

- Solver
- Data Import/Export
- Optimization
- Diagnostics
  - Sample Time
  - Data Validity
  - Type Conversion
  - Connectivity
  - Compatibility
  - Model Referencing
  - Saving
- Hardware Implementation
- Model Referencing
- Simulation Target
  - Symbols
  - Custom Code
- Real-Time Workshop
  - Report
  - Comments
  - Symbols
  - Custom Code
  - Debug
  - Interface
- HDL Coder
  - Global Settings
  - Test Bench
  - FPGA Tool Scripts

### Simulation time

Start time: 0.0

Stop time: 10.0

### Solver options

Type: Fixed-step

Solver: discrete (no continuous states)

Fixed-step size (fundamental sample time):

auto

### Tasking and sample time options

Periodic sample time constraint:

Unconstrained

Tasking mode for periodic sample times:

Auto

Constrain model's discrete sample times to specified values.

☐ Automatically handle rate transition for data transfer

☐ Higher priority value indicates higher task priority

OK

Cancel

Help

Apply

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### Target selection

System target file: rtwin.tlc

Browse...

Language: C

Description: Real-Time Windows Target

### Build process

Compiler optimization level: Optimizations on (faster runs)

TLC options:

### Makefile configuration

☒ Generate makefile

Make command: make\_rtw

Template makefile: rtwin.tmf

Select rtwin.tlc

### Code Generation Advisor

Select objective: Unspecified

Check model before generating code: Off

Check model ...

Specify whether to check model before build.

☐ Generate code only

Build

OK

Cancel

Help

Apply